WHAT IS CLAIMED IS:

1. A cache memory system comprising:

a main memory configured to hold at least one data entry in a first location;

a cache memory comprising:

a cache data memory configured to hold the data entry; and

a cache tag memory configured to store a first main memory address of the data entry; and

a processor configured to reassign the data entry from the first location to a second location in the main memory by overwriting the cache tag memory with a second main memory address without modifying the data entry in the cache data memory.

2. The cache memory system of Claim 1, wherein the processor is further configured to mark the data entry in the cache data memory as having been modified.

3. The cache memory system of Claim 1, wherein the main memory is comprised of a DRAM circuit.

4. The cache memory system of Claim 1, wherein the processor and the cache memory are on the same integrated circuit.

5. The cache memory system of Claim 1 further comprising a memory controller configured to perform a snoop cycle.

6. The cache memory system of Claim 1, wherein the cache data memory is further configured to hold the data entry in multiple cache lines.

7. The cache memory system of Claim 1, wherein the data entry is written to the second location in the main memory if the cache tag memory has been modified.

8. The cache memory system of Claim 1, wherein the data entry is written to the second location in the main memory if the data entry has been marked modified.

9. The cache memory system of Claim 1, wherein the act of writing the data entry occurs before the second location in the main memory is accessed for the data entry.

10. A method of reassigning data from a first memory location to a second memory location comprising writing a value to an entry in a cache tag memory without changing the content of an entry in a cache data memory associated with said entry in said cache tag memory.

11. The method of Claim 10, additionally comprising marking said entry in said cache data memory as having been modified.

12. The method of Claim 10, wherein the entry in the cache data memory corresponds to a portion of the data being reassigned from the first memory location to the second memory location.

13. The method of Claim 10, wherein the cache data memory is fully associative.

14. The method of Claim 10, wherein the first memory location corresponds to a location in a main memory.

15. The method of Claim 14, wherein the main memory is comprised of a DRAM circuit.

16. The method of Claim 10, wherein writing the value to the entry in the cache tag memory is controlled by a processor.

17. The method of Claim 16, wherein the processor and the cache data memory are on the same integrated circuit.

18. The method of Claim 10 further comprising performing a snoop cycle.

19. The method of Claim 10, wherein the cache data memory is further configured to store the entry in multiple cache lines.

20. The method of Claim 10 further comprising writing the entry to the second memory location if the cache tag memory has been modified.

21. The method of Claim 10 further comprising writing the entry to the second memory location if the entry in the cache data memory has been marked modified.

22. The method of Claim 21, wherein writing the entry to the second memory location occurs before the second memory location is accessed for the entry.

23. A cache memory system for performing virtual data movement within a digital processing system, the system comprising:

a main memory configured to hold at least one data string in a first location;

a cache memory comprising:

a cache data memory configured to hold the data string; and

a cache tag memory associated with the cache data memory, the cache tag memory configured to store a first main memory address corresponding to the first location of the data string; and

a processor configured to receive an instruction to move the data string from the first location to a second location in the main memory, the processor being further configured to overwrite the cache tag memory with a second main memory address without modifying the data string in the cache data memory.

24. The cache memory system of Claim 23, wherein the processor is further configured to mark the data string in the cache data memory as having been modified.

25. The cache memory system of Claim 23, wherein the processor further comprises:

a first execution unit configured to receive, decode and perform assembly language arithmetic and logic instructions; and

a second execution unit configured to receive, decode and perform assembly language string manipulation instructions, wherein the second execution unit is separate from the first execution unit.

26. The cache memory system of Claim 25, wherein the second execution unit is configured to operate without intervention of the first execution unit.

27. The cache memory system of Claim 23, wherein the main memory is comprised of a DRAM circuit.

28. The cache memory system of Claim 23, wherein the processor and the cache memory are on the same integrated circuit.

29. The cache memory system of Claim 23 further comprising a memory controller configured to perform a snoop cycle.

30. The cache memory system of Claim 23, wherein the cache data memory is further configured to store the data string in multiple cache lines.

31. The cache memory system of Claim 23, wherein the data string is written to the second location in the main memory if the cache tag memory has been modified.

32. The cache memory system of Claim 23, wherein the data string is written to the second location in the main memory if the data string has been marked modified.

33. The cache memory system of Claim 32, wherein the act of writing the data string occurs before the second location in the main memory is accessed for the data string.

34. A method for virtual data movement in a cache memory system within a digital processing system, the method comprising:

storing a data string in a first main memory location;

storing the data string in a cache data memory;

storing in a cache tag memory a first address corresponding to the first main memory location;

receiving an instruction to move the data string from the first main memory location to a second main memory location; and

overwriting the cache tag memory with a second address corresponding to the second main memory location without changing the content of the data string in the cache data memory.

35. The method of Claim 34 further comprising marking the data string in the cache data memory as having been modified.

36. The method of Claim 34 further comprising:

receiving a second instruction to access the data string at the second main memory location;

verifying if the data string is stored in the cache data memory and if the data string has been marked modified; and

writing the data string to the second main memory location if the data string has been marked modified.

37. The method of Claim 34, wherein the cache data memory is fully associative.

38. The method of Claim 34, wherein the main memory is comprised of a DRAM circuit.

39. The method of Claim 34, wherein the instruction to move the data string is received by a processor.

40. The method of Claim 39, wherein the processor and the cache data memory are on the same integrated circuit.

41. The method of Claim 34 further comprising performing a snoop cycle.

42. The method of Claim 34, wherein the cache data memory is further configured to store the data string in multiple cache lines.

43. The method of Claim 34 further comprising writing the data string to the second main memory location if the cache tag memory has been modified.

44. The method of Claim 34 further comprising writing the data string to the second main memory location if the data string in the cache data memory has been marked modified.

45. The method of Claim 44, wherein writing the data string to the second main memory location occurs before the second main memory location is accessed for the data string.

46. A cache system comprising:

main memory means for storing a data entry at a first main memory location;

cache memory means for storing the data entry;

cache tag means for storing the first main memory location of the data entry; and

processing means for receiving an instruction to move the data entry from the first main memory location to a second main memory location, said processing means configured to overwrite the first main memory location in the cache tag means with the second main memory location in response to receiving said instruction without moving the data entry in the cache memory means.

47. The cache system of Claim 46 further comprising a memory controller means for performing a snoop cycle.

48. The cache system of Claim 46, wherein the cache memory means is further configured to store the data entry in multiple cache lines.

49. The cache system of Claim 46, wherein the processing means is further configured to mark the data entry in the cache memory means as having been modified.

50. The cache system of Claim 46, wherein the main memory means is comprised of a DRAM circuit.

51. The cache system of Claim 46, wherein the processing means and the cache memory means are on the same integrated circuit.

52. The cache system of Claim 46, wherein the data entry is written to the second main memory if the cache tag means has been modified.

53. The cache system of Claim 46, wherein the data entry is written to the second main memory location if the data entry has been marked modified.

54. The cache system of Claim 53, wherein the act of writing the data entry occurs before the second main memory location is accessed for the data entry.

55. A method for data manipulation in a digital processing system, the method comprising:

storing a block of data at a first series of addresses in a main memory;

storing the block of data in multiple cache lines of a cache data memory;

storing in a cache tag memory associated with the cache data memory the first series of addresses corresponding to the location of the block of data in the main memory;

receiving an instruction with a processor to move the block of data from the first series of addresses to a second series of addresses in the main memory; and

overwriting the cache tag memory with the second series of addresses without changing the content of the block of data in the cache data memory.

56. The method of Claim 55 further comprising marking each cache line wherein the block of data is stored as having been modified.

57. The method of Claim 55, wherein the step of receiving said instruction with the processor to move the block of data further comprises:

receiving said instruction at a first execution unit within the processor; and

routing said instruction to a second execution unit within the processor, said second execution unit being separate from the first instruction unit.

58. The method of Claim 55 further comprising performing a snoop cycle before accessing the block of data at the second series of addresses.

59. The method of Claim 55 further comprising:

receiving a second instruction to access the block of data at the second series of addresses in the main memory;

verifying if the block of data is stored in the cache data memory and if the cache lines wherein the block of data is stored have been marked modified; and

writing the block of data to the second series of addresses in the main memory if the cache lines have been marked modified.

60. The method of Claim 55 further comprising writing the block of data to the second series of addresses in the main memory based on a write through policy.

61. The method of Claim 55, wherein the cache data memory is fully associative.

62. The method of Claim 55, wherein the main memory is comprised of a DRAM circuit.

63. The method of Claim 55, wherein the processor and the cache data memory are on the same integrated circuit.

64. The method of Claim 55 further comprising performing a snoop cycle.

65. The method of Claim 55 further comprising writing the block of data to the second series of addresses in the main memory if the cache tag memory has been modified.

66. The method of Claim 55 further comprising writing the block of data to the second series of addresses in the main memory if a cache line wherein a portion of the block of data is stored has been marked modified.

67. The method of Claim 66, wherein writing the block of data to the second series of addresses in the main memory occurs before the second series of addresses in the main memory is accessed for the block of data.